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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,420	CHEN ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *1-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-32* is/are rejected.

7)☒ Claim(s) *32 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/01/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 03/01/2004 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention II, claims 18-33, in the reply filed on 06/14/2005 is acknowledged.

3. Claims 1-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse, as noted above.

Claim Objections

4. **Claim 32** is objected to because of the following informalities: Dependency of claim 32 is not proper. Correct dependency of claim 32 so as to provide proper antecedent bases for "the first layer" and "the second layer". For examination purposes, claim 32 is treated as being dependent on claim 31. Appropriate correction is required.

Claim 33 is objected to because of the following informalities: Claim 33 appears to contain a typographical error. The "first" in "the first silicide region is substantially aligned with the fourth sidewall spacer" (line 5) should have been "second" because that is what is disclosed in the detailed description.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 18, 23, and 25-27** are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. U.S. Patent Application Publication 20020164847 (the '847 reference).

The '847 reference discloses in Figures 1-18 and respective portions of the specification a method as claimed.

Referring to **claim 18**, the reference discloses a method comprising:

providing a substrate (100, Fig. 13);

forming, over the substrate, a first gate (110) for an N-channel transistor (in the NMOS Region) and a second gate (110) for a P-channel transistor;

forming a first sidewall spacer (the vertical portion of layer 130 or 120, Fig. 14) for the N-channel transistor lateral to the first gate and a second sidewall spacer (130 or 120) for the P-channel transistor lateral to the second gate;

forming a third sidewall spacer (140, Fig. 14) for the N-channel transistor lateral to the first sidewall spacer and a fourth sidewall spacer (150) for the P-channel transistor lateral to the second sidewall spacer;

providing a first mask (370, Fig. 16) over the first gate;

implanting dopants, while the first mask is over the first gate, of a first conductivity type (p-type) into the substrate;

removing the first mask (Fig. 18) after the implanting the dopants of the first conductivity type;

providing a second mask (380, Fig. 18) over the second gate;

implanting dopants, while the second mask is over the second gate, of a second conductivity type (n-type) into the substrate; and

removing the third sidewall spacer (140) while the second mask (380) is over the second gate (paragraph [0040]: "A third photo-resist pattern 380 exposing the NMOS region is then formed. The spacers 140 remaining on the side walls of the gate electrodes 110 in the NMOS region are then removed").

Referring to **claim 23**, the reference further discloses that the providing the first mask (370, Fig. 16) occurs prior to the providing the second mask (380, Fig. 18).

Referring to **claim 25**, the reference further discloses:

implanting dopants in a first region (generally defined by 364, Fig. 18) and a second region (no number, formed with a similar dimension as region 364) of the substrate of the second conductivity type for forming a first extension (364) and a second extension (no number) for the N-channel transistor, respectively; and

implanting dopants in a third region (374) and a fourth region (no number, formed with a similar dimension as region 374) of the substrate of the first conductivity type for forming a third extension (374) and a fourth extension (no number) for the P-channel transistor, respectively.

Referring to **claim 26**, the reference further discloses:

the implanting dopants in the substrate of the second conductivity type are utilized to form a first doped region (362) and a second region (no number, formed with a similar dimension as region 362) in the substrate that are in contact with the first extension (364) and second extension, respectively; and

the implanting dopants of the first conductivity type are utilized to form a third doped region (372) and a fourth doped region (no number, formed with a similar dimension as region 372) in the substrate in contact with the third extension (374) and the fourth extension, respectively.

Referring to **claims 18 and 27**, the reference also discloses a method comprising:

providing a substrate (100, Fig. 1);

forming, over the substrate, a first gate (110) for an N-channel transistor (in the NMOS Region) and a second gate (110) for a P-channel transistor;

forming a first sidewall spacer (the vertical portion of layer 130 or 120, Fig. 14) for the N-channel transistor lateral to the first gate and a second sidewall spacer (130 or 120) for the P-channel transistor lateral to the second gate;

forming a third sidewall spacer (140, Fig. 14) for the N-channel transistor lateral to the first sidewall spacer and a fourth sidewall spacer (150) for the P-channel transistor lateral to the second sidewall spacer;

providing a first mask (170, Fig. 5) over the first gate;

implanting dopants, while the first mask is over the first gate, of a first conductivity type (p-type) into the substrate;

removing the first mask after the implanting the dopants of the first conductivity type (the removing the first mask after the implanting the dopants of the first conductivity type is not shown but must happen for the final product to function);

providing a second mask (160, Fig. 3) over the second gate;

implanting dopants, while the second mask is over the second gate, of a second conductivity type (n-type) into the substrate;

removing the third sidewall spacer (140, Fig. 4) while the second mask (160) is over the second gate; and

implanting dopants, while the second mask (160) is over the second gate and after removing the third sidewall spacer (140), of the second conductivity type into the substrate (Fig. 4).

6. **Claim 18 and 27** are rejected under 35 U.S.C. 102(b) as being anticipated by Check et al. U.S. Patent 6,316,302 (the '302 reference).

The '302 reference discloses in Figures 1-4 and respective portions of the specification a method as claimed.

Referring to **claim 18**, the reference discloses a method comprising:

providing a substrate (10, Fig. 1);

forming, over the substrate, a first gate (22) for an N-channel transistor (in the NMOS Region) and a second gate (22) for a P-channel transistor;

forming a first sidewall spacer (24b or 24a) for the N-channel transistor lateral to the first gate and a second sidewall spacer (24b or 24a) for the P-channel transistor lateral to the second gate;

forming a third sidewall spacer (24c) for the N-channel transistor lateral to the first sidewall spacer and a fourth sidewall spacer (24c) for the P-channel transistor lateral to the second sidewall spacer;

providing a first mask (26) over the first gate;

implanting dopants, while the first mask is over the first gate, of a first conductivity type (p-type) into the substrate;

removing the first mask (Fig. 2) after the implanting the dopants of the first conductivity type;

providing a second mask (30 or 38, Fig. 2 or Fig. 4) over the second gate;

implanting dopants, while the second mask (30 or 38) is over the second gate, of a second conductivity type (n-type) into the substrate; and

removing the third sidewall spacer (24c) while the second mask (30 or 38) is over the second gate (Fig. 2 or Fig. 4).

Referring to **claim 27**, the reference further discloses implanting dopants, while the second mask (38) is over the second gate and after removing the third sidewall spacer (24c), of the second conductivity type into the substrate (Fig. 4).

7. **Claim 18 and 27-28** are rejected under 35 U.S.C. 102(b) as being anticipated by Krivokapic et al. U.S. Patent 6,512,273 (the '273 reference).

The '273 reference discloses in Figures 1 and 2A-2D and respective portions of the specification a method as claimed.

Referring to **claim 18**, the reference discloses a method comprising:

providing a substrate (2, Fig. 2A);

forming, over the substrate, a first gate (10) for an N-channel transistor (in the n-channel region 14, column 4, lines 38-67) and a second gate (10) for a P-channel transistor (region 4);

forming a first sidewall spacer (18, Fig. 2B) for the N-channel transistor lateral to the first gate and a second sidewall spacer (18) for the P-channel transistor lateral to the second gate;

forming a third sidewall spacer (20) for the N-channel transistor lateral to the first sidewall spacer and a fourth sidewall spacer (33/34, Fig. 2D) for the P-channel transistor lateral to the second sidewall spacer;

providing a first mask (step 52 – Fig. 1, column 4, lines 55-60) over the first gate;

implanting dopants, while the first mask is over the first gate, of a first conductivity type (p-type, from BF2, step 54) into the substrate;

removing the first mask (step 56) after the implanting the dopants of the first conductivity type;

providing a second mask (step 66, column 5, lines 1-25) over the second gate;

implanting dopants (step 72), while the second mask is over the second gate, of a second conductivity type (n-type) into the substrate (the second mask is to be removed in step 76); and

removing the third sidewall spacer (20, step 70, column 5, lines 5-10) while the second mask is over the second gate (the second mask is to be removed in step 76).

Referring to **claim 27**, the reference further discloses implanting dopants (in step 74, while the second mask (formed in step 66) is over the second gate and after removing the third sidewall spacer (20, step 70), of the second conductivity type into the substrate (Fig. 4).

Referring to **claim 28**, the reference further discloses that the first gate comprises polysilicon (column 4, line 46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 24 and 28-30** are rejected under 35 U.S.C. §103(a) as being unpatentable over Kim et al. U.S. Patent Application Publication 20020164847 (the '847 reference).

Referring to **claim 24**, the reference discloses that the providing the first mask (370, Fig. 16) occurs prior to the providing the second mask (380, Fig. 18) as claimed in claim 23 and as detailed above. Therefore, it can not be said that the providing the first mask (370, Fig. 16) occurs after the providing the second mask (380, Fig. 18) as claimed. However, it appears that changing the sequence does not result in a different product, therefore the change would have been obvious to one of ordinary skill in the art.

Referring to **claims 28 and 29**, although the reference fails to disclose that the first gate, which must be an electrical conductive gate for the device to function, comprises polysilicon, and fails to disclose that the first gate, which must be an electrical conductive gate for the device

to function, comprises metal, polysilicon and metal were at the time the invention was made available conductive materials that one of ordinary skill in the art would use, therefore would have been obvious, to form electrical conductive gates. As for the limitation of claim 30, a silicon on an insulator (SOI) substrate offers advantage over a plain silicon substrate as is known in the art, therefore the change from a simple substrate to an SOI substrate would have been obvious.

9. **Claims 19-21** are rejected under 35 U.S.C. §103(a) as being unpatentable over Kim et al. U.S. Patent Application Publication 20020164847 (the '847 reference) in view of Grudowski U.S. Patent Application Publication 20050020022 or in view of Haselden et al. U.S. Patent Application Publication 20040014305.

The '847 reference discloses a method as claimed and as detailed above and further discloses forming a first liner (the vertical portion of layer 120, Fig. 13) over the first gate and a second liner (120) over the second gate prior to the forming the first sidewall spacer (130) and the second sidewall spacer (130), but fails to teach forming a third liner over the first sidewall spacer and a fourth liner over the second sidewall spacer prior to the forming the third sidewall spacer (140) and the fourth sidewall spacer (140). The third sidewall spacer (140), as detailed above and as claimed, is eventually etched in another step.

Grudowski, in also disclosing a method for forming an etched sidewall spacer, teaches that in forming the etched sidewall spacer, the etched sidewall spacer should be a silicon nitride layer and further teaches that the nitride layer, which is equivalent to the third sidewall spacer,

should be formed over an oxide liner, which is equivalent to the third liner, so that when the etched sidewall spacer is etched, the liner functions as an effective etch stop (paragraph [0027]).

Haselden, in also disclosing a method for forming an etched sidewall spacer, teaches that in forming the etched sidewall spacer, the etched sidewall spacer should be a silicon nitride layer and further teaches that the nitride layer, which is equivalent to the third sidewall spacer, should be formed over an oxide liner, which is equivalent to the third liner, so that when the etched sidewall spacer is etched, the liner functions as an etch stop (paragraph [0009]).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's device such that a third liner over the first sidewall spacer and a fourth liner over the second sidewall spacer prior to the forming the third sidewall spacer (140) and the fourth sidewall spacer (140). One would have been motivated to make such a change because the additional liner functions as an etch stop as taught by Grudowski or Haselden.

10. **Claims 31-32** are rejected under 35 U.S.C. §103(a) as being unpatentable over Kim et al. U.S. Patent Application Publication 20020164847 (the '847 reference) in view of Grudowski U.S. Patent Application Publication 20050020022 or in view of Haselden et al. U.S. Patent Application Publication 20040014305 and further in view of Joh U.S. Patent 5,580,804.

As detailed above for claims 19-21, the '847 reference's method modified in view of Grudowski or Haselden comprises forming the third liner over the first sidewall spacer and the fourth liner over the second sidewall spacer prior to the forming the third sidewall spacer (140) and the fourth sidewall spacer (140), both of which should be a nitride, thereby meeting the

limitation that the second layer includes nitride. As for the limitation that the first layer includes nitride, the '847 reference teaches forming a first layer 130 including a nitride (paragraph [0036]) that is to become the first sidewall spacer 130 and the second sidewall spacer 130.

However, the combined teachings fail to disclose that forming the respective sidewall spacers 130 and 140 is by a dry etching after forming the first layer 130 and the second layer 140.

Joh, in also disclosing a method for etching sidewall spacers, teaches that etching sidewall spacers is preferably dry etching because preferable spacer forms are achieved (column 5, lines 50-62).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to etch the reference's sidewalls using a dry etching process. One would have been motivated to make such a change because dry etching enables preferable shapes for the sidewalls.

11. **Claim 22** is rejected under 35 U.S.C. §103(a) as being unpatentable over Krivokapic et al. U.S. Patent 6,512,273 (the '273 reference) in view of Komori et al. U.S. Patent 6,847,080.

The '273 reference discloses a method as claimed and as detailed above including a first contact region to make electrical contact with the doped region 36/35' in the substrate for the N-channel transistor so as the N-channel transistor could be utilized in an integrated circuit, wherein the first region is a first distance from the first gate (Fig. 2D), and a second contact region to make electrical contact with the doped region 26/28' in the substrate for the P-channel transistor so as the P-channel transistor could be utilized in an integrated circuit, wherein the

second region is a second distance from the second gate (Fig. 2D), and wherein the second distance is greater than the first distance.

Komori, in also disclosing a method comprising forming a gate on a substrate and forming a doped region in the substrate, teaches siliciding the contact region of the doped region, which is also known as a source/drain region, so that the resulting transistor achieve lower contact resistance and higher speed (column 12, first paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to modify the '273 reference's method to include the siliciding step of the contact regions of the source drain regions. One would have been motivated to make such a change in view of the teachings in Komori that siliciding the contact region of the doped regions results in transistor having a lower contact resistance and a higher speed.

Allowable Subject Matter

12. Claim 33 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten to overcome the claim objection noted above.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a method as recited in claim 33, characterized in forming a first sidewall spacer, forming a third sidewall spacer, removing the third sidewall spacer, forming a first silicide region in the substrate for the N-channel transistor, and forming a second silicide region in the substrate for

the P-channel transistor, the first silicide region being substantially aligned with the first sidewall spacer and the second silicide region being substantially aligned with the fourth sidewall spacer.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
July 06, 2005